

**Notice of References Cited**

Application/Control No.

09/752,576

Applicant(s)/Patent Under  
Reexamination  
KHARE ET AL.

Examiner

Thang H Ho

Art Unit

2188

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,737,568	04-1998	Hamaguchi et al.	711/121
	B	US-5,222,224	06-1993	Flynn et al.	711/144
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	James Archibald and Jean-Loup Baer, Cache Coherence Protocols: Evaluation Using a Multiprocessor Simulation Model, ACM Transactions on Computer Systems, November 1986, Vol.4, No. 4, Pages 273-298
	V	James Archibald and Jean-Loup Baer, An Economical Solution to the Cache Coherence Problem, IEEE, 1984, Pages 355-362
	W	Paruvachi V. Raja and Subramaniam Ganesan, A Hardware Cache Coherency Scheme For Multiprocessors, IEEE, 1993, Pages 181-184
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.